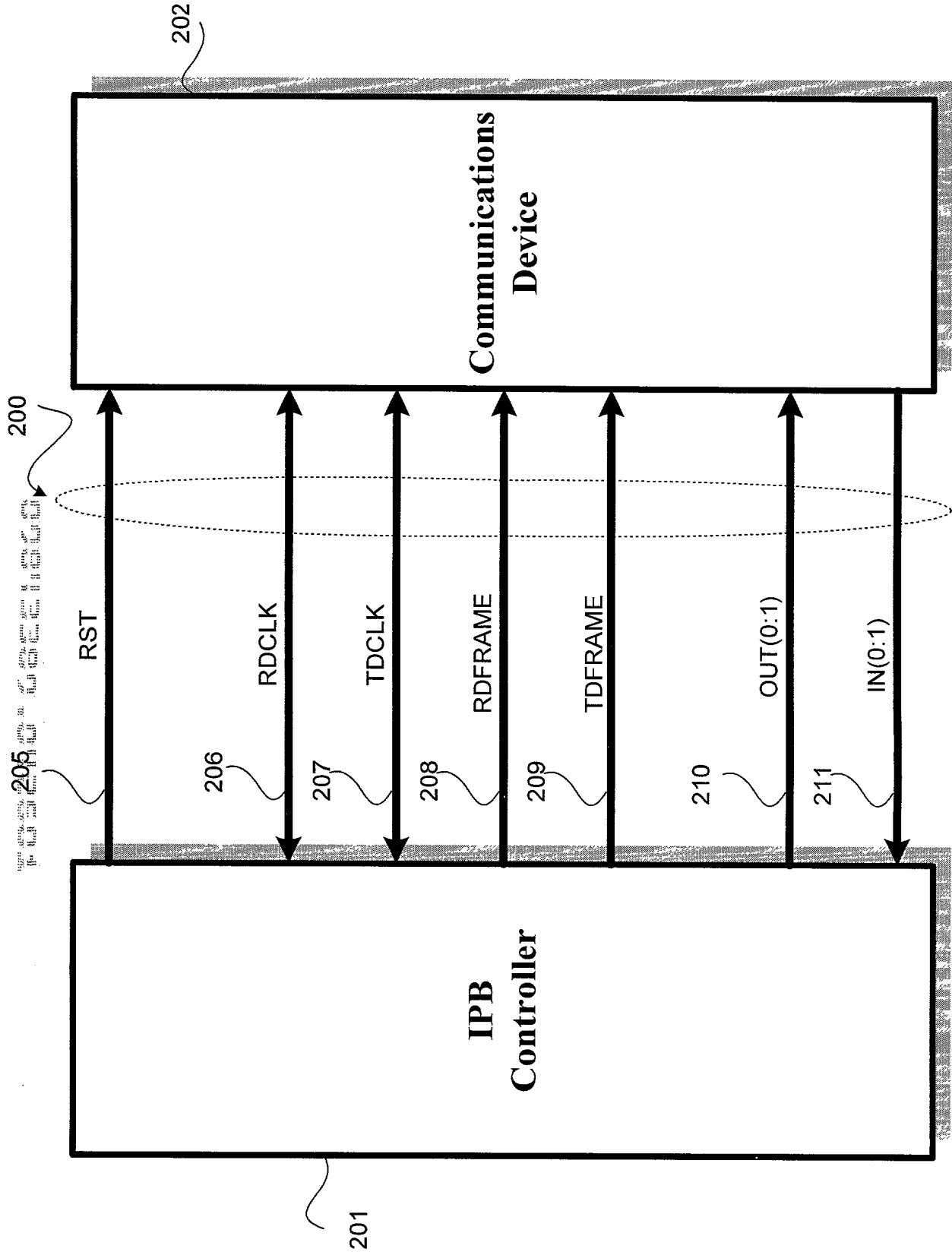
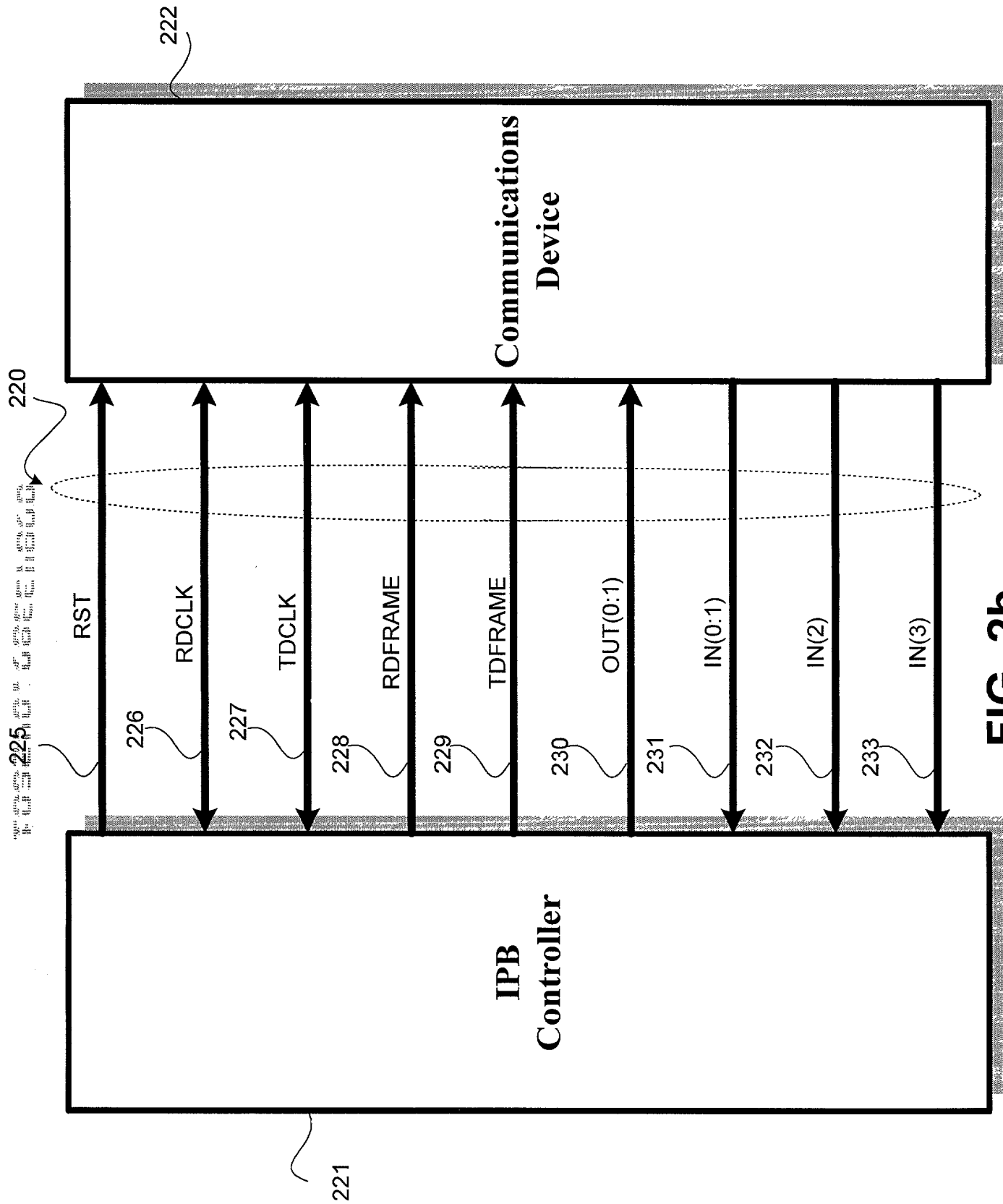


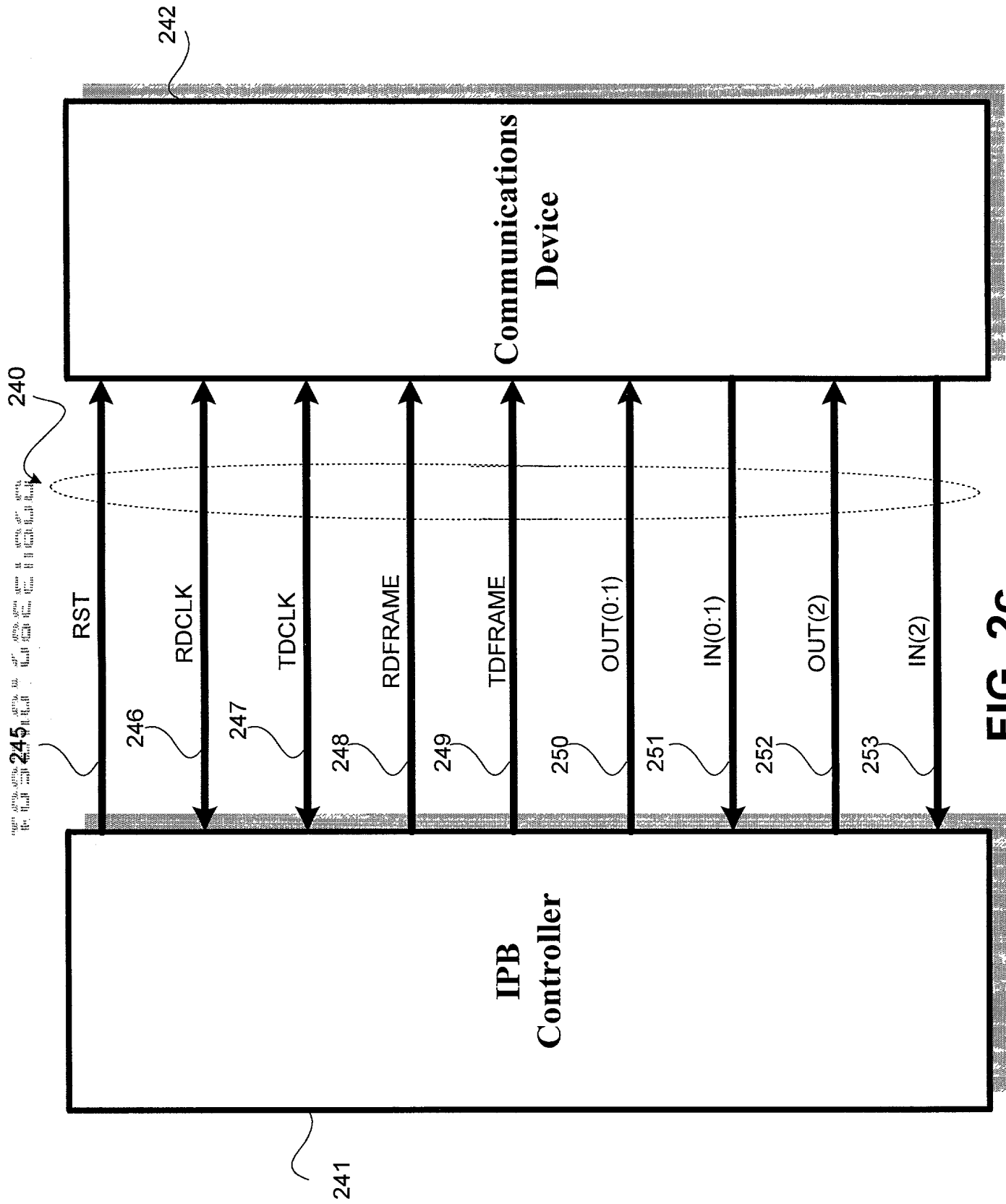
FIG. 1



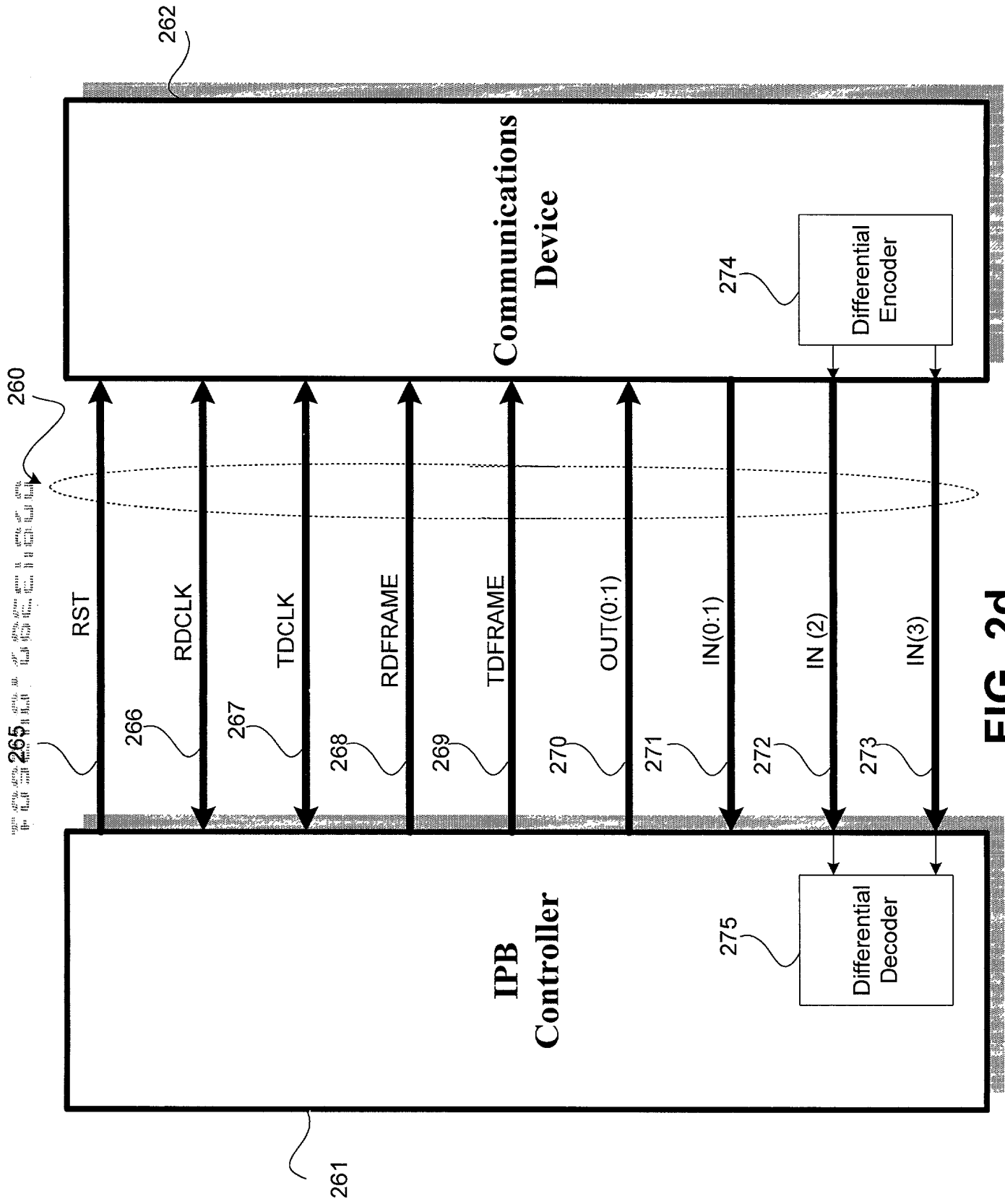
**FIG. 2a**



**FIG. 2b**



**FIG. 2c**



**FIG. 2d**

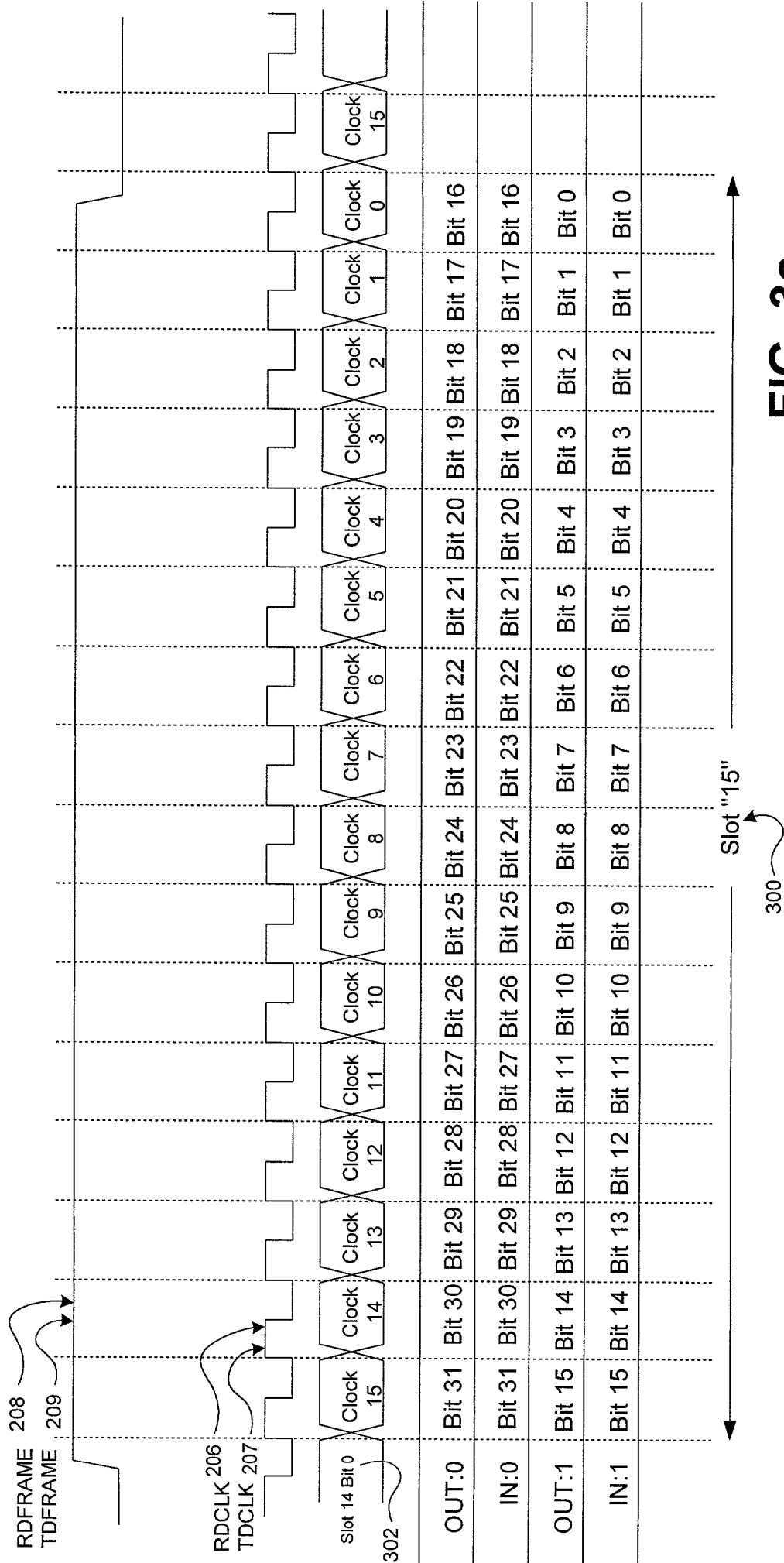


FIG. 3a

FIG. 3b is a timing diagram illustrating the relationship between the RDCLK 206 and TDCLK 207 signals and the data transfer process. The diagram shows the RDCLK 206 and TDCLK 207 signals, the data transfer process, and the resulting data transfer results. The data transfer process is shown as a series of data transfer operations, each corresponding to a specific clock cycle. The resulting data transfer results are shown as a series of data transfer results, each corresponding to a specific clock cycle.

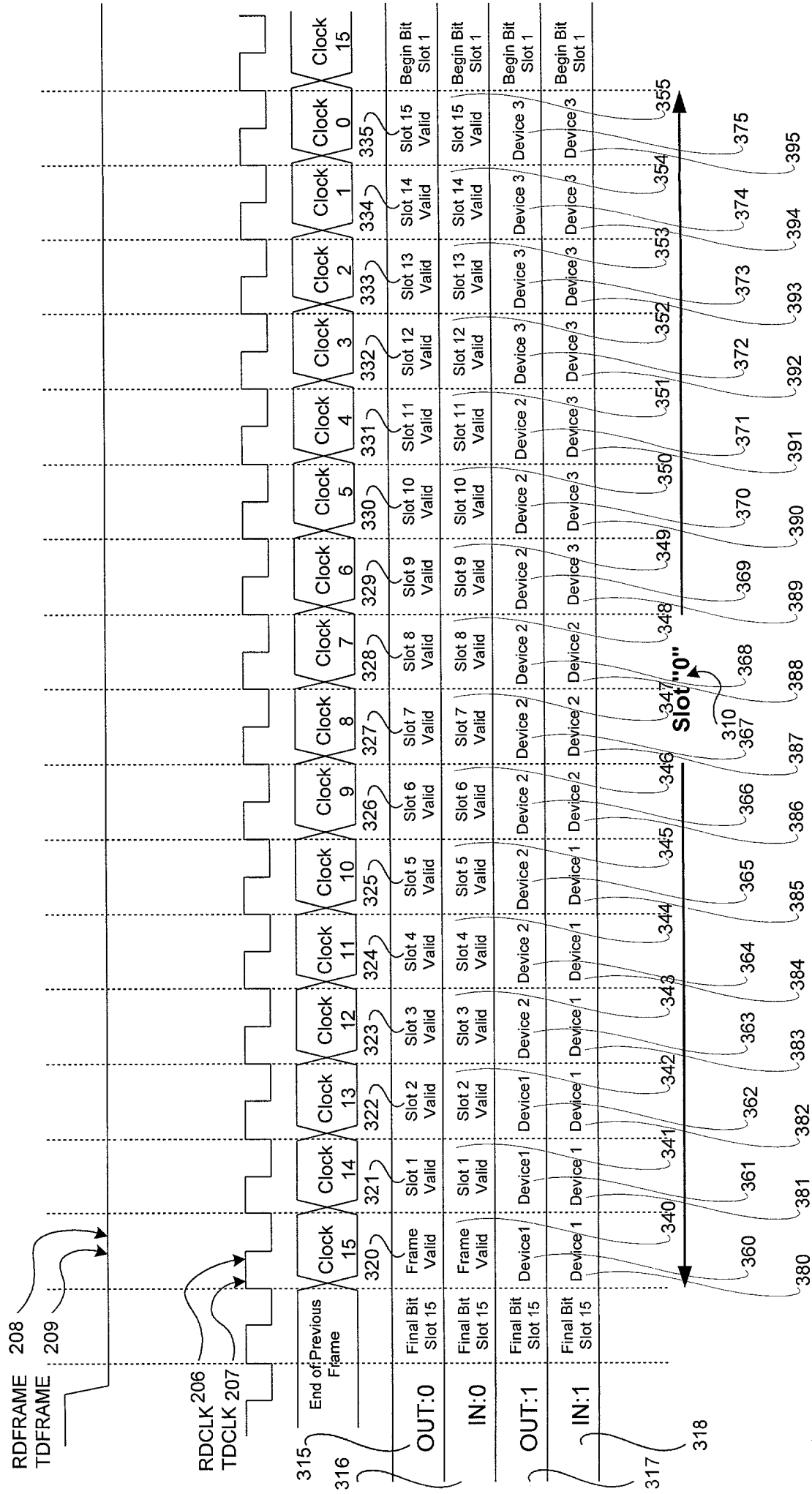


FIG. 3b

FIG. 3C is a timing diagram illustrating the relationship between the RDCLK 226, TDCLK 227, and the RDFRAME 228, TDFRAME 229 signals. The diagram shows that the RDCLK 226 and TDCLK 227 signals are clock signals that are phase-shifted relative to each other. The RDFRAME 228 and TDFRAME 229 signals are frame signals that are also phase-shifted relative to each other. The diagram illustrates that the RDCLK 226 and TDCLK 227 signals are used to clock the RDFRAME 228 and TDFRAME 229 signals, respectively.

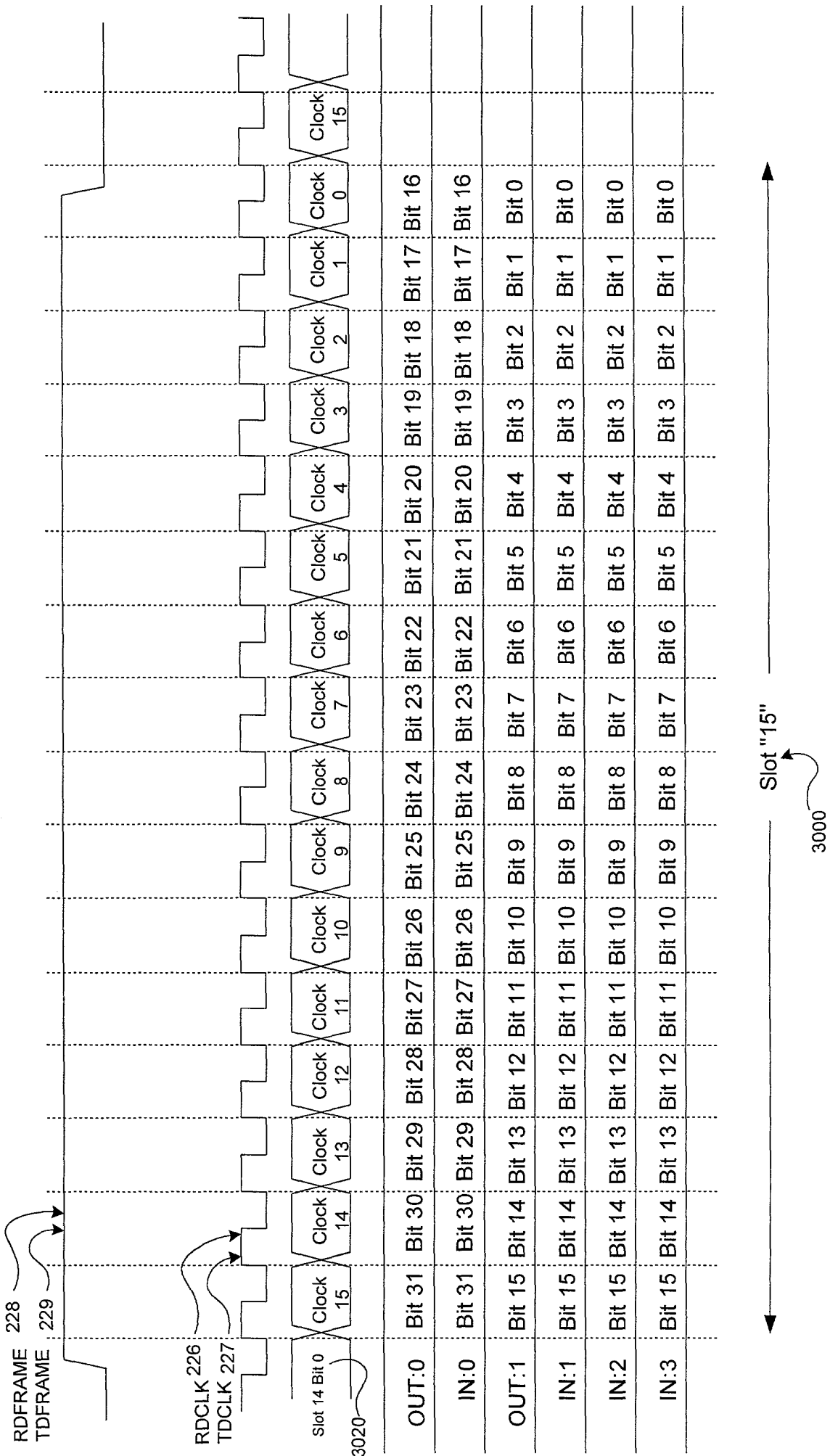


FIG. 3C



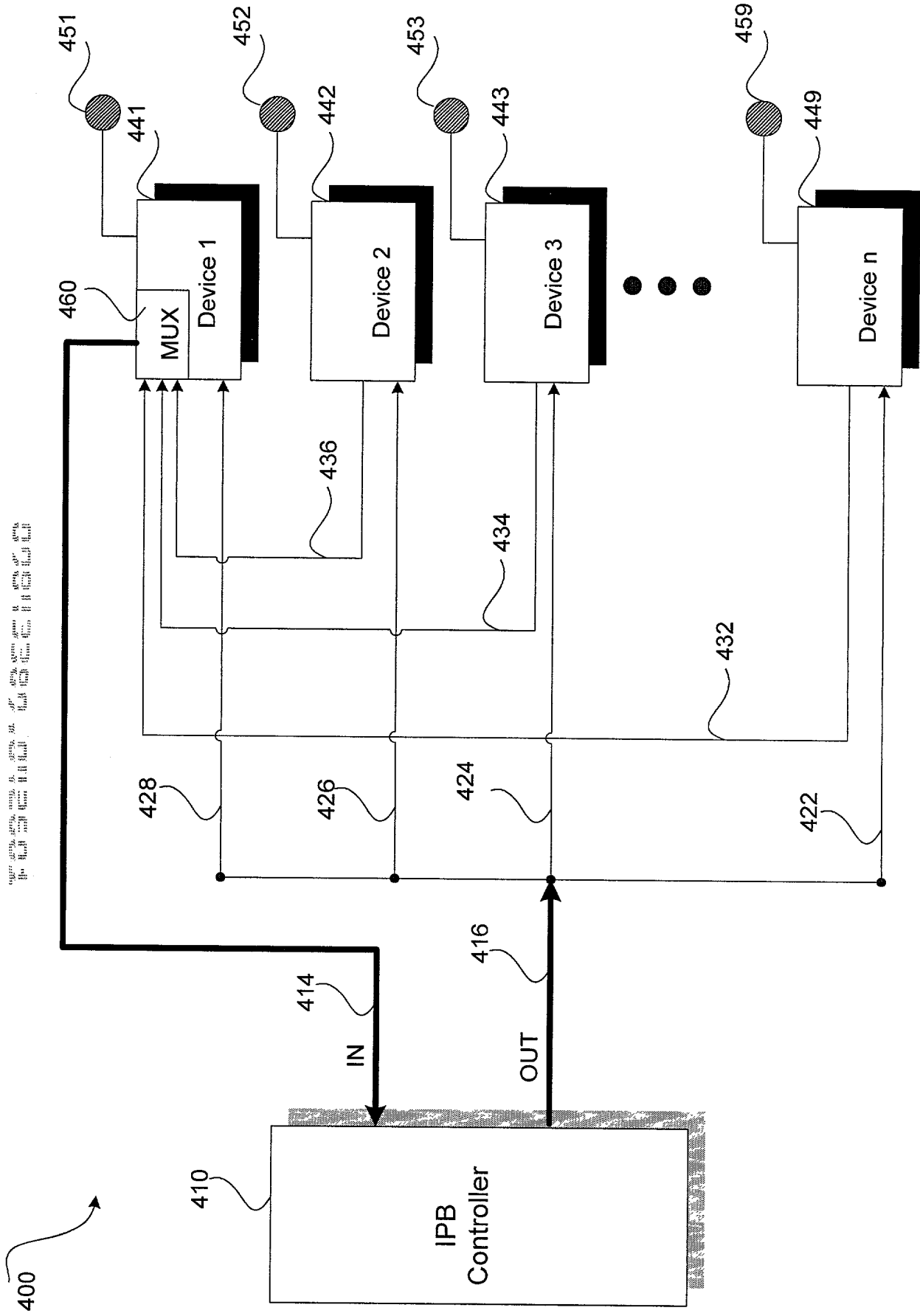
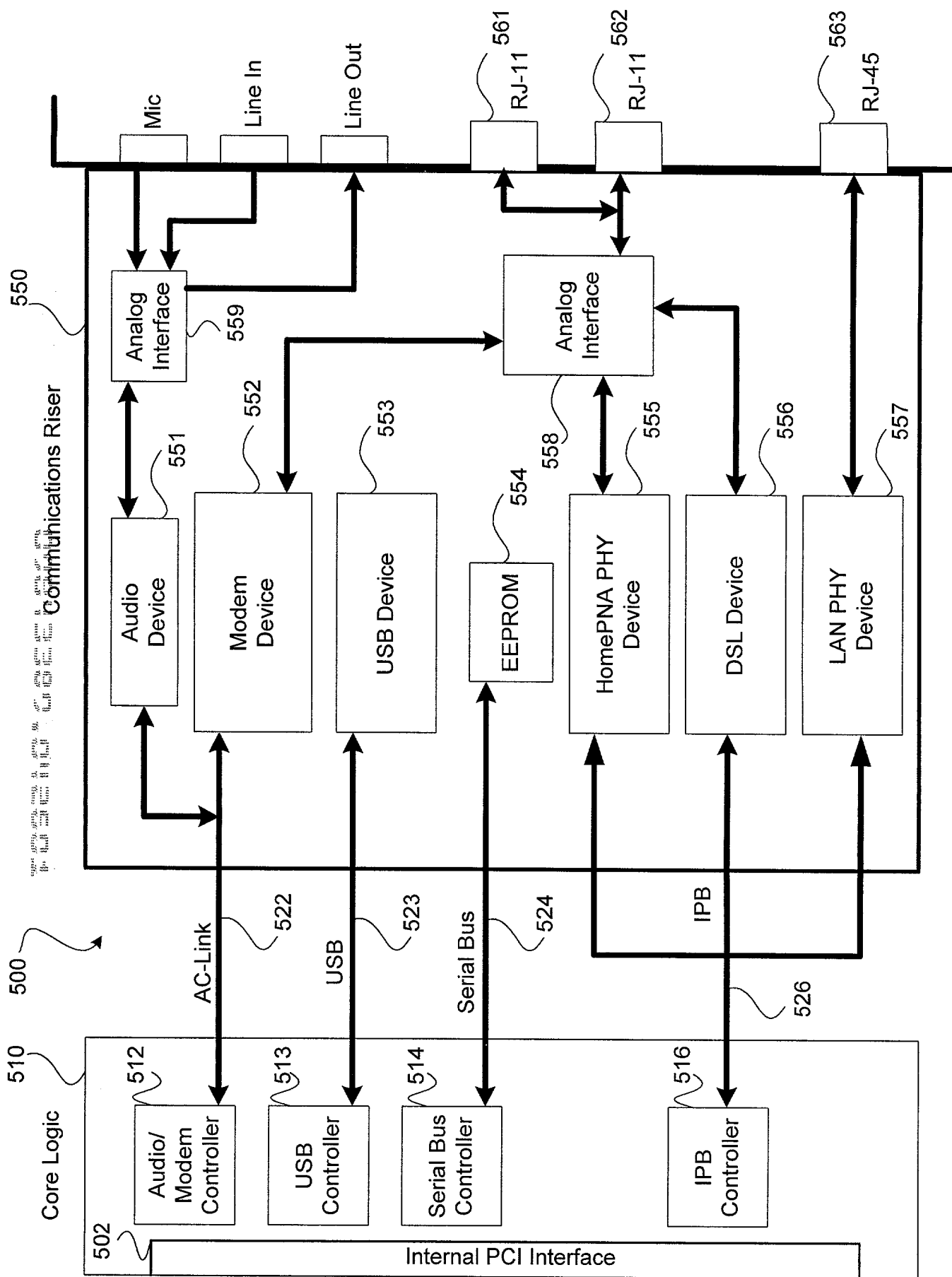


FIG. 4



**FIG. 5**